

Features

- Operating voltage:
 - 2.4V~5V for the HT12A/B/C
 - 2.4V~12V for the HT12E
- Low power and high noise immunity CMOS technology
- Low stand-by current
- Minimum transmission word:
 - Four words for the HT12E
 - One word for the HT12A/B/C

Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers

General Description

- A built-in oscillator with only a 5% resistor
- HT12A/B/C with a 38KHz carrier for Infra-Red transmission medium
- Data code polarity: - HT12A/C/E: Positive polarity - HT12B: Negative polarity
- Minimal external components
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

The 2¹² encoders are a series of CMOS LSIs for remote control system applications. They are capable of encoding information which consists of N address bits and 12–N data bits. Each address/data input can be set to one of the two logic states. The programmed addresses/data are transmitted together with the header bits

Selection Table

via an RF or an Infra-Red transmission medium upon receipt of a trigger signal. The capability to select a TE trigger on the HT12E or a DATA trigger on the HT12A/B/C further enhances the application flexibility of the 2¹² series of encoders. The HT12A/B/C additionally provides a 38KHz carrier for Infra-Red systems.

Function Item	Address No.	Address/ Data No.	Data No.	Oscillator	Trigger	Package	Carrier Output	Negative Polarity
HT12A	8	0	4	455K Hz resonator	D8~D11	18 DIP/ 20 SOP	38K Hz	No
HT12B	8	0	4	455K Hz resonator	D8~D11	18 DIP/ 20 SOP	38K Hz	Yes
HT12C	0	0	10	455K Hz	D2~D11	16 DIP/ 16 SOP	38K Hz	No
111120	2	0	10	resonator		18 DIP		110
HT12E	8	4	0	RC oscillator	TE	18 DIP/ 20 SOP	No	No

Note: Address/Data represents pins that can be address or data according the decoder requirement.

15th Mar '96



Block Diagram

TE trigger

HT12E



DATA trigger

HT12A/B/C



Note: The address data pins are available in various combinations (refer to the address/data table).

2



Pin Description

Pin Name	I/O	Internal Connection	Description
A0 A7	T	CMOS IN Pull-High (HT12A/B/C)	Input pins for address A0~A7 setting
A0~A7	1	NMOS TRANSMISSION GATE (HT12E)	They can be externally set to VDD or VSS.
AD8~AD11	Ι	NMOS TRANSMISSION GATE (HT12E)	Input pins for address/data AD8~AD11 setting They can be externally set to VDD or VSS (only for the HT12E).
D2~D11	Ι	CMOS IN Pull-High	Input pins for data D2~D11 setting and transmission enable, active low They can be externally set to VSS or left open (see Note).
DOUT	0	CMOS OUT	Encoder data serial transmission output
L/MB	Ι	CMOS IN Pull-High	Latch/Momentary transmission format selection pin: Latch: Floating or VDD Momentary: VSS
TE	Ι	CMOS IN Pull-High	Transmission enable, active low (see Note).
OSC1	Ι	OSCILLATOR 1	Oscillator input pin
OSC2	0	OSCILLATOR 1	Oscillator output pin
X1	Ι	OSCILLATOR 2	455KHz resonator oscillator input
X2	0	OSCILLATOR 2	455KHz resonator oscillator output
VSS	Ι	_	Negative power supply (GND)
VDD	Ι	—	Positive power supply

Note: D2~D11 are all data input and transmission enable pins of the HT12A/B/C.

3

 $\overline{\text{TE}}$ is a transmission enable pin of the HT12E.



Approximate internal connection circuits



Absolute Maximum Ratings

Supply Voltage (HT12A/	B/C)–0.3V to 5.5V
Input Voltage	$V_{SS}0.3$ to $V_{DD}\mbox{+-}0.3V$
Operating Temperature.	–20°C to 75°C

Supply Voltage (HT12E)	0.3V to 13V
Storage Temperature	–50°C to 125°C

Electrical Characteristics

1T12A/B/C (Ta=25°								
	D		Test Condition	Min	T		T	
Symbol	Parameter	VDD	Condition	Min.	Typ.	Max.	Unit	
VDD	Operating Voltage	_	_	2.4	3	5	V	
Tama	Stand by Compart	3V	Ossillatan atana	_	0.1	1	μA	
ISTB	Stand-by Current	5V	Oscillator stops.	_	0.1	1	μA	
T	Operating Current	3V No	No load	_	200	400	μA	
IDD	Operating Current	5V	Fosc=455KHz	_	400	800	μA	
Ter a sum	Output Drive Comment	5V	V _{OH} =0.9V _{DD} (Source)	-1	-1.6	_	mA	
IDOUT	Output Drive Current	31	V _{OL} =0.1V _{DD} (Sink)	2	3.2		mA	
VIH	"H" Input Voltage	_	_	0.8V _{DD}	_	VDD	V	
V _{IL}	"L" Input Voltage	_	_	0	_	$0.2V_{DD}$	V	
RDATA	D2~D11 Pull-High Resistance	5V	V _{DATA} =0V	_	150	300	KΩ	

15th Mar '96



HT12E

(Ta=25°C)

Shal	Demonster		Test Condition	M	T	Mari	T I #4
Symbol	Parameter	V _{DD}	Condition	win.	тур.	Max.	Unit
V _{DD}	Operating Voltage	_	_	2.4	5	12	V
Tama	Stand by Cumpont	3V	Occillator store	_	0.1	1	μΑ
ISTB	Stand-by Current	12V	Oscillator stops.	_	2	4	μΑ
T	O	3V	No load	_	40	80	μΑ
IDD	Operating Current	12V	F _{OSC} =3KHz	_	150	300	μA
T	Output Drive Current	5 V	V _{OH} =0.9V _{DD} (Source)	-1	-1.6	_	mA
IDOUT	Output Drive Current	эv	V _{OL} =0.1V _{DD} (Sink)	1	1.6	_	mA
VIH	"H" Input Voltage	_	_	0.8V _{DD}	_	Vdd	V
VIL	"L" Input Voltage	_	_	0	_	$0.2V_{DD}$	V
Fosc	Oscillator Frequency	5V	Rosc=1.1MΩ	_	3	_	KHz
RTE	TE Pull-High Resistance	5V	V _{TE} =0V	_	1.5	3	MΩ



Functional Description

Operation

The 2^{12} series of encoders begins a 4 word transmission cycle upon receipt of a transmission enable (TE for the HT12E or D2~D11 for the HT12A/B/C, active low). This cycle will repeat itself as long as the transmission enable (TE or D2~D11) is held low. Once the transmission enable returns high the encoder output completes its final cycle and then stops as shown in Fig.1 for the HT12E and in Fig.2,3 for the HT12A/B/C.





Fig.3 Transmission timing for the HT12A/B/C (L/MB=VSS)

Information word

L/MB is the Latch/Momentary type selection pin. If L/MB=1 the device is in the latch mode (for use with the latch type of data decoders). When the transmission enable is removed during a transmission, the DOUT pin outputs a complete word and then stops. On the other hand, if L/MB=0 the device is in the momentary mode (for use with the momentary type of data decoders). When the transmission enable is removed during a transmission, the DOUT outputs a complete word and then adds 7 words all with the "1" data code.

An information word consists of 3 periods as illustrated in Fig.4.



Fig.4 Composition of information

6



Address/data waveform

Each programmable address/data pin can be externally set to one of the following two logic states as shown in Fig.5 (for the HT12E) and Fig.6,7 (for the HT12A/B/C):



Fig.5 Address/Data bit waveform for the HT12E



Fig.6 Address/Data bit waveform for the HT12A/C

The HT12B data code polarity is inverted:



Fig.7 Address/Data bit waveform for the HT12B

The address/data bits of the HT12A/B/C are transmitted with a 38KHz carrier for Infra-Red remote controller flexibility.

7



Address/data programming (preset)

The status of each address/data pin can be individually pre-set to logic "high" or "low". If a transmission enable signal is applied, the encoder scans and transmits the status of the 12 bits of address/data serially in the order A0 to AD11 for the HT12E encoder and A0 to D11 for the HT12A/B/C encoder.

During information transmission these bits are transmitted with a preceding synchronization bit. But if the trigger signal is not applied, the chip enters the stand-by mode and consumes a reduced current which is less than $1\mu A$ for a supply voltage of 5V.

Usual applications preset the address pins with individual security codes by the DIP switches or PCB wiring, while the data is selected by the push button or electronic switches.

The following figure shows an application using the HT12E:



The transmitted information is as shown:

Pilot	A0	A1	A2	A3	A4	A5	A6	A7	AD8	AD9	AD10	AD11
& Sync	1	0	1	0	0	0	1	1	1	1	1	0
Sync.	1	U	1	U	U	U	1	1	1	1	1	U

Address/Data sequence

The following provides a table of the address/data sequence for various models of the 2¹² series encoders. A correct device should be selected according to the requirements of individual address and data.

HOLTEK		Address/Data Bits											
Part No.	0	1	2	3	4	5	6	7	8	9	10	11	
HT12A	A0	A1	A2	A3	A4	A5	A6	A7	D8	D9	D10	D11	
HT12B	A0	A1	A2	A3	A4	A5	A6	A7	D8	D9	D10	D11	
HT12C	A0	A1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	
HT12E	A0	A1	A2	A3	A4	A5	A6	A7	AD8	AD9	AD10	AD11	

8



Transmission enable

For the HT12E encoder, transmission is enabled by applying a low signal to the $\overline{\text{TE}}$ pin. But for the HT12A/B/C encoders transmission it is enabled by applying a low signal to one of the data pins D2~D11.

9

Flowchart

HT12A/B/C





Note: D2~D11 are transmission enables of the HT12A/B/C.

 $\overline{\text{TE}}$ is the transmission enable of the HT12E.



Oscillator frequency chart of the HT12E



15th Mar '96



Package Information

8 Address		8 Address		8 Address 4 Data		
			,			
· · · · ·	,	NC 1	20□NC		71	
A0 🗖 1 🔾		A0 🗖 2		A0 🗖 1 🔪		
A1 🗖 2	17 DOUT	A1 🗖 3	18DOUT	A1 🗖 2	17 DOUT	
A2 🗖 3	16 🗆 X1	A2 🗖 4	17 X1	A2 🗖 3	16口X1	
A3 🗖 4	15 🗆 X2	A3 🗖 5	16 口 X2	A3 🗖 4	15 🗆 X2	
A4 🗖 5	14 🗆 L/MB	A4 🗖 6	15 🗖 L/MB	A4 🗖 5	14 🗖 L/МВ	
A5 🗖 6	13 🗆 D11	A5 🗖 7	14口D11	A5 🗖 6	13口D11	
A6 🗖 7	12 🗖 D10	A6 🗖 8	13口D10	A6 🗖 7	12 🗖 D10	
A7 🗖 8	11 🗖 D9	A7 🗖 9	12口D9	A7 🗖 8	11 🗖 D9	
vss⊏l 9	10 🗆 D8	VSS 🗖 10	11 🗖 D8	VSS 🗖 9	10 🗆 D8	
HT1	24	HT1	2A	HT12B		
-18	DIP	- 20 \$	SOP	– 18 DIP		
8 Address		0 Address		2 Address		
8 Address 4 Data		0 Address 10 Data		2 Address 10 Data		
8 Address 4 Data	20-100	0 Address 10 Data		2 Address 10 Data		
8 Address 4 Data		0 Address 10 Data		2 Address 10 Data		
8 Address 4 Data NC 1 A0 2 A1 3	20 DNC 19 DVDD 18 DOUT	0 Address 10 Data		2 Address 10 Data		
8 Address 4 Data NC 1 A0 2 A1 3 A2 4	20 DNC 19 DVDD 18 DOUT 17 X1	0 Address 10 Data	16 □ DOUT	2 Address 10 Data A0 1 A1 2 D2 3	18 VDD 17 DOUT 16 X1	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5	20 DNC 19 DVDD 18 DOUT 17 DX1 16 DX2	0 Address 10 Data	16 DOUT 15 DX1 14 X2	2 Address 10 Data A0 1 A1 2 D2 3 D3 4	7 18 VDD 17 DOUT 16 X1 15 X2	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5 A4 6	20 DNC 19 DVDD 18 DOUT 17 X1 16 X2 15 L/MB	0 Address 10 Data VDD 1 D2 2 D3 3 D4 4	16 DOUT 15 X1 14 X2 13 U/MB	2 Address 10 Data A0 1 A1 2 D2 3 D3 4 D4 5	7 18 UDD 17 DOUT 16 X1 15 X2 14 U MB	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5 A4 6 A5 7	20 DNC 19 DVDD 18 DOUT 17 X1 16 X2 15 L/MB 14 D11	0 Address 10 Data VDD 1 D2 2 D3 3 D4 4 D5 5	16 DOUT 15 X1 14 X2 13 L/MB 12 D11	2 Address 10 Data A0 1 A1 2 D2 3 D3 4 D4 5 D5 6	18 UDD 17 DOUT 16 X1 15 X2 14 L/MB 13 D11	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5 A4 6 A5 7 A6 8	20 DNC 19 VDD 18 DOUT 17 X1 16 X2 15 L/MB 14 D11 13 D10	0 Address 10 Data VDD 1 D2 2 D3 3 D4 4 D5 5 D6 6	16 □ DOUT 15 □ X1 14 □ X2 13 □ L/MB 12 □ D11 11 □ D10	2 Address 10 Data A0 [1 A1 [2 D2] 3 D3 [4 D4 [5 D5 [6 D6 [7	18 UDD 17 DOUT 16 X1 15 X2 14 L/MB 13 D11 12 D10	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5 A4 6 A5 7 A6 8 A7 9	20 DNC 19 VDD 18 DOUT 17 X1 16 X2 15 L/MB 14 D11 13 D10 12 D9	0 Address 10 Data VDD 1 D2 2 D3 3 D4 4 D5 5 D6 6 D7 7	16 DOUT 15 X1 14 X2 13 L/MB 12 D11 11 D10 10 D9	2 Address 10 Data A0 [1 A1 [2 D2 [3 D3 [4 D4 [5 D5 [6 D6 [7 D7 [8]	18 UDD 17 DOUT 16 X1 15 X2 14 L/MB 13 D11 12 D10 11 D9	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5 A4 6 A5 7 A6 8 A7 9 VSS 10	20 DNC 19 VDD 18 DOUT 17 X1 16 X2 15 L/MB 14 D11 13 D10 12 D9 11 D8	0 Address 10 Data VDD [1 D2 [2 D3 [3 D4 [4 D5 [5 D6 [6 D7 [7 VSS [8	16 DOUT 15 X1 14 X2 13 L/MB 12 D11 11 D10 10 D9 9 D8	2 Address 10 Data A0 [1 A1 [2 D2] 3 D3 [4 D4 [5 D5 [6 D6 [7 D7 [8 VSS [9]	18 UDD 17 DOUT 16 X1 15 X2 14 L/MB 13 D11 12 D10 11 D9 10 D8	
8 Address 4 Data NC 1 A0 2 A1 3 A2 4 A3 5 A4 6 A5 7 A6 8 A7 9 VSS 10 HT1	20 NC 19 VDD 18 DOUT 17 X1 16 X2 15 L/MB 14 D11 13 D10 12 D9 11 D8 28	0 Address 10 Data VDD [1 D2 [2 D3 [3 D4 [4 D5 [5 D6 [6 D7 [7 VSS [8	16 DOUT 15 X1 14 X2 13 L/MB 12 D11 11 D10 10 D9 9 D8 20	2 Address 10 Data A0 [1 A1 [2 D2] 3 D3 [4 D4 [5 D5 [6 D6 [7 D7 [8 VSS [9	18 VDD 17 DOUT 16 X1 15 X2 14 L/MB 13 D11 12 D10 11 D9 10 D8 20	

15th Mar '96



8	Address
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_		1					
A0 🗖 1	14						
A1 🗖 2	13						
A2□3	12	□OSC1					
A3 🗖 4	11	□OSC2					
A4□5	10	I TE					
A5 □ 6	9	⊐vss					
A6 □ 7	8	DA7					
HT12E - 14 DIP							

8 Address	
2 Address/Data	l

		,			
A0 🗆	1	í 16			
A1 □	2	15	DOUT		
A2 🗆	3	14	DOSC1		
A3 🗆	4	13	⊐osc2		
A4 □	5	12	DTE		
A5 🗆	6	11	DAD11		
A6 🗆	7	10	DAD10		
A7 🗆	8	9	⊐vss		
HT12E					
– 16 SOP					

12

8 Address 4 Address/Data					
A0 🗆	1	18 UDD			
A1 🗆	2	17 DOUT			
A2 🗆	3	16 OSC1			
A3 🗆	4	15 OSC2			
A4 🗆	5	14 🗆 TE			
A5 🗆	6	13 🗆 AD11			
A6 🗆	7	12 🗖 AD10			
A7 🗆	8	11 🗖 AD9			
VSS 🗆	9	10 🗆 AD8			
HT12E – 18 DIP					

8 Address 4 Address/Data

Address/Data						
1	20	Бис				
2	19					
3	18	□ропт				
4	17	DOSC1				
5	16	⊐osc2				
6	15					
7	14	DAD11				
8	13	DAD10				
9	12	AD9				
10	11	DAD8				
HT12E - 20 SOP						
	1 2 3 4 5 6 7 8 9 10 HT12 – 20 SC	1 20 2 19 3 18 4 17 5 16 6 15 7 14 8 13 9 12 10 11 HT12E - 20 SOP				



Application circuit 2

Application Circuits

Application circuit 1



Note: Typical infrared diode: EL-1L2 (KODENSHI CORP.) Typical RF transmitter: JR-220 (JUWA CORP.) TX-99 (MING MICROSYSTEM, U.S.A.) FD-493TX (FISCHER-OLSEN, GERMANY).

13